Claims

1. A system comprising:

a processor (180);

a plurality of register bank blocks (120, 121, 122, 123, 124, 125); and,

a register bank block decoder circuit (140) for activating one and only one of the plurality of register bank blocks (120, 121, 122, 123, 124, 125), the register bank block decoder circuit (140) responsive to interrupt event operations for selecting the one of the plurality of register bank blocks (120, 121, 122, 123, 124, 125) for being activated, where different interrupt event operations result in selection of different ones of the plurality of register bank blocks (120, 121, 122, 123, 124, 125).

2. A system according to claim 1, comprising:

a memory circuit (182) for storing of a first program data and for storing of a second program data associated with a second interrupt priority,

wherein the processor (180) is for utilizing a first register bank block (120) from the plurality of register bank blocks (120, 121, 122, 123, 124, 125) during execution of the first program stream, and for upon the occurrence of an interrupt resulting from an interrupt event associated with the second program stream, executing the second program stream utilizing the second register bank block (121), the second register bank block (121) different and logically isolated from the first register bank block (120).

3. A system according to claim 2, wherein the second program stream has a higher interrupt priority than the first program stream.

4. A system according to claim 1, comprising:

an input data bus (151); and,

an input switching circuit (131, 132, 133, 134) coupled to the plurality of register bank blocks (120, 121, 122, 123, 124, 125) and having a selection input port for receiving a register bank selection signal from the register bank block decoder circuit (140), the input switching circuit (131, 132, 133, 134) for activating one of the plurality of register bank blocks (120, 121, 122, 123, 124, 125) in dependence upon the register bank selection signal, the activated one of the plurality of register bank blocks (120, 121, 122, 123, 124, 125) for being coupled to the input data bus (151).

5. A system according to claim 4, wherein the input switching circuit (131, 132, 133, 134) is a multiplexer circuit.

6. A system according to claim 4, comprising:

an output data bus (152); and,

an output switching circuit (111, 112, 113, 114) coupled to the plurality of register bank blocks and having a selection input port for receiving the register bank block selection signal from the register bank block decoder circuit (140), the output switching circuit (111, 112, 113, 114) for switchably coupling the activated one of the plurality of register bank blocks (120, 121, 122, 123, 124, 125) to the output data bus (152).

7. A system according to claim 6, wherein the output switching circuit (111, 112, 113, 114) is a multiplexer circuit.

8. A system according to claim 6, comprising a circuit (140a) for storing and retrieving of bank block selection data derived from the register bank block selection signal of a pre interrupt switch state, wherein upon terminating of an interrupt event the input switching circuit (131, 132, 133, 134) and the output switching circuit (111, 112, 113, 114) is provided with the pre interrupt register bank block selection signal derived from the stored bank block selection data.

9. A system according to claim 8, wherein the state of the circuit (140a) for storing and retrieving of the register bank block selection signal is based on interrupt priority

10. A system according to claim 6, wherein the register bank block selection signal is based solely on interrupt priority.

11. A system according to claim 1, wherein a first register bank block (120) from the plurality of register bank blocks (120, 121, 122, 123, 124, 125) is concurrently enabled along with a second different register bank block (121, 122, 123, 124, 125) from the plurality of register bank blocks (120, 121, 122, 123, 124, 125), the second different register bank block (121, 122, 123, 124, 125) independently addressable from the first register bank block (120).

12. A system according to claim 1, comprising a debug bank select register (150) coupled to the register bank block decoder circuit (140), the debug bank select register (150) for providing access to data stored within the plurality of register bank blocks (120, 121, 122, 123, 124, 125) during a step of debugging.

13. A method of switching processing resources in a data processing system comprising the steps of:

providing a plurality of register bank blocks (120, 121, 122, 123, 124, 125);

utilizing (1101) a first register bank block (120) from the plurality of register bank blocks (120, 121, 122, 123, 124, 125) for data processing;

receiving (1102) of an interrupt request for initiating an interrupt event;

determining (1103) if the interrupt request is to be fulfilled, and if so, then:.

selecting (1104) a second register bank block (121) from the plurality of register bank blocks (120, 121, 122, 123, 124, 125),

the selected second register bank block (121) in isolation from the first register bank block (120); and,

utilizing (1105) the second register bank block (121) from the plurality of register bank blocks (120, 121, 122, 123, 124, 125) for data processing.

14. A method according to claim 13, wherein a first program stream is provided for utilizing of the first register bank block (120) and a second program stream is provided for utilizing the second register bank block (121).

15. A method according to claim 14, the first program stream has a lower interrupt priority than the second program stream, the interrupt priority used in the step of determining (1103) whether to fulfill the interrupt request.

16. A method according to claim 14, comprising the step of:
providing a processor (180) for executing of the first and second program streams.

17. A method according to claim 16, comprising the step of:
halting (1112) execution of the second program stream;
selecting (1113) the first register bank block; and,
resuming (1114) execution of the first program stream.

18. A method according to claim 17, wherein executing the instructions of the second program stream takes place without altering the contents of the first register bank block (120) in suspended use by the first program stream.

19. A method according to claim 13, comprising the step of:
providing a memory circuit (182) having a first memory region for storing of program stream data related to the first program stream.

20. A method according to claim 14, wherein the first and second program streams other than have stored therein instruction data for storing and restoring of register bank block (120, 121, 122, 123, 124, 125) contents.

21. A storage medium having data stored thereon, the data for implementation of a processing system comprising:

first instruction data for providing a plurality of register bank blocks (120, 121, 122, 123, 124, 125); and,

second instruction data for providing a register bank block decoder circuit (140) for activating one of the plurality of register bank blocks (120, 121, 122, 123, 124, 125) in isolation, the register bank block decoder circuit (140) responsive to interrupt event operations for selecting the one of the plurality of register bank blocks (120, 121, 122, 123, 124, 125) for being activated, where different interrupt event operations result in selection of different ones of the plurality of register bank blocks (120, 121, 122, 123, 124, 125).